FPGA Based Phase Gradient Controller for Phased Array Radar Antenna

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***Abstract*:**
The paper presents the architecture of the phase gradient controller for phased array Radar antenna. It assists in dispersing the phase gradients to individual elements and steer the beam in the desired volume. The paper depicts detailed hardware and software methodology adopted during the development.

Keywords: FPGA, Phase, Attenuation, Controller

I. INTRODUCTION

Antenna is a structure to provide transition from guided wave to free space wave and vice versa. It acts as a transducer and impedance match between the transmitter and the propagation medium (space) and between the medium and receiver. It provides gain to concentrate the transmitted power in a preferred direction. It also provides the area, called as aperture, to intercept and capture received echoes [1].

Antenna is an inherent part of any Radar system. Scanning Radars are classified into two major categories, mechanical steered antenna and electronically steered antenna. The electronic scanning or inertia less scanning uses a group of radiating elements with the relative phases of the respective signals feeding the elements such that the effective radiation pattern of the array is reinforced in a desired direction [2].

In Active Electronically Scanned Array antenna, the RF energy distribution and beam steering logic are present in the same limited space. For accurate beam steering it is required to compute and apply the phase gradients in azimuth (and elevation) for each of the element. Therefore, the Phase Gradient Controller (PGC) must meet following objectives:

- *Fine control over each antenna element*
- *Least beam switching time*
- *Smallest distribution delay*
- *Synchronization of all the components*
- *Optimum timing and resource utilization*

Radar antenna consists of transmit/receive (T/R) modules connected to the radiating elements (panels), beam steering network consisting of controllers and their interconnections, RF distribution network, calibration (CAL) distribution network and power supply. All these antenna electronics is integrated to form a mechanical frame assembly. This paper presents FPGA based design for the phase gradient controller to steer beam in the desired direction.

Section II introduces a typical architecture of Radar. The proposed system is presented in Section III. Section IV gives details on features incorporated in the design. Section V and VI gives test results and conclusion respectively.

II. BACKGROUND

Phase Gradient Controller is an integral part of the phased array Radar system that can be deployed for surveillance using mast or a tripod.

As shown in figure 1, T/R microwave modules are the key elements of the active phased array Radar [3]. Large numbers of individual T/R modules are integrated with the respective radiating elements to ensure a great degree of redundancy. They are responsible for the generation of transmit power, low noise amplification, phase shift and provides an appropriate interface between the array beam steering controller and the radiating elements. Three major functional blocks of a T/R module are: RF block, digital & power conditioning and interconnects & packaging.

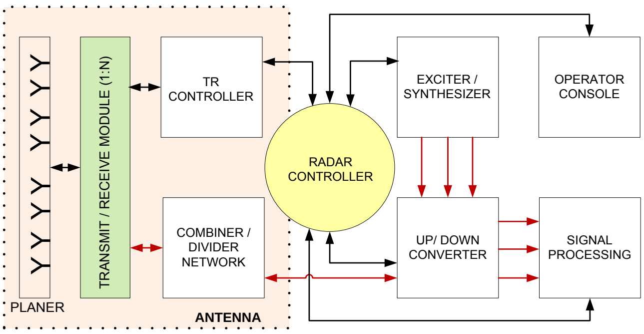

Figure 1: System Block Diagram

The PGC provides interface between T/R module and the Radar controller (RC). It consists of power conditioning & distribution block to deliver current during pulsed operation, control signals for attenuation & phase control switching at every Pulse Repetition Time (PRT) and calibration of T/R modules.

III. PROPOSED SYSTEM

To interface the large number of T/R modules in phased array architecture, FPGA based beam steering controller is found optimum. It computes the phase, amplitude and timing generation for each T/R module. Efficient software is designed to enable antenna scan the desired volume of interest without glitches or errors. The design is modular and can be adapted for variety of phased array Radar antennas.

Once the desired volume of interest is selected by the operator, OC (Operator Console) communicates 'look angle' to the RC. RC plans ahead the future beam position and accordingly communicates the common phase gradient data for all the radiating elements. PGC receives this data, computes the position-wise phase values for each element, caters for the calibration error and applies it to the individual elements on the panel. The parameters received during a burst are stored in BRAMs (Block RAMs) of FPGA and applied during next burst.

As shown in the figure 2, the PGC suffice the needs of power supply filtering, generation of different DC voltages and phase - amplitude calculations & correction for T/R modules.

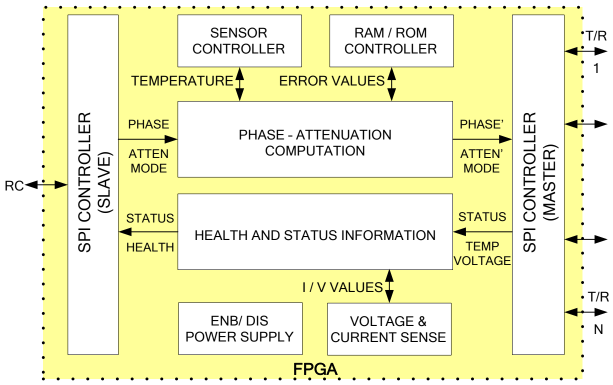

Figure 2: Functional Block Diagram of PGC

Considering an array of (m, n) elements, the phase of the individual element is represented as:

$$Phase\ (m,n) = m * P_A + n * P_B \qquad \text{(i)}$$

where (m, n) are the indices of the individual antenna channel, P_A is the phase gradient in the azimuth and P_B is the phase gradient in the elevation.

The phase gradients are represented as:

$$P_A = (\pi / \lambda) * dh * Sin(az) * Cos(el) \qquad \text{(ii)}$$

$$P_B = (\pi / \lambda) * dv * Sin(az) * Sin(el) \qquad \text{(iii)}$$

where 'az' is steering angle azimuth, 'el' is steering angle elevation, 'λ' is wavelength of the EM wave being used, 'dh' is the element spacing in azimuth and 'dv' is element spacing in elevation.

Advantages of proposed design are:

- *Highly flexible and re-programmable*
- *Capability for parallel processing*
- *Small design cycle*
- *Lower design cost*

IV. DESIGN METHODOLOGY

A. Modes of Operation

Three different modes of operation are provided to encompass the complete system requirement. These modes are:

1) Normal Mode: During this mode, RC calculates phase gradients from the required 'look angle' for a given azimuth and elevation. PGC receives these gradients and computes phase attenuation values for all the channels. It applies corresponding error correction values from the error table. Updates computed values to the individual T/R modules.

2) Calibration Mode: Calibration is performed to estimate the phase and attenuation errors between the antenna elements. These errors can occur due to the change in operating environment like temperature. During this mode, the error tables used in the normal mode of operation is updated. It is performed in two parts: Transmit Calibration and Receive Calibration.

a) Transmit Calibration: During this mode, one of the transmit channel is enabled at a time and all the other channels are disabled. Same phase and attenuation values are applied to individual antenna elements one by one. Actual phase at the radiation element is measured using dedicated CAL channel. The channel variations are stored as transmit error table.

b) Receive Calibration: During this mode, one channel is enabled at a time and all other channels are disabled. CAL antenna is used to transmit waveform with fixed phase and attenuation. Actual values are measured at each channel. The deviation from channel to channel is stored as receive error table.

3) Status Mode: During this mode, status of individual T/R modules, power supplies, temperature and other information are periodically monitored to ensure proper functionality of the Radar. This information is gathered from individual T/R elements and communicated to RC. It is presented to the operator using Graphics User Interface (GUI) on the OC. A dedicated Ethernet channel is provided for detailed troubleshooting wherein online data can be captured and monitored.

B. Hardware Design

As shown in figure 3, the proposed design is built around Cyclone V FPGA [4].

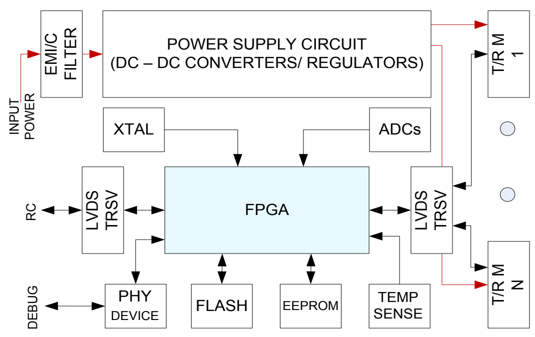

Figure 3: PGC Hardware Architecture

It uses an onboard clock, Analog to Digital Convertors (ADC), power supply conditioning & monitoring circuitry, multiple trans-receivers, memory and PHY device. It uses Serial Peripheral Interface (SPI) bus [5] to interface with RC over Low Voltage Differential Signaling (LVDS) voltage levels [6]. Similarly, SPI bus is provided to communicate between the hardware and T/R modules.

C. Software Design

The proposed design has three major software modules:

1) SPI Slave Module: This software section provides interface between PGC and RC over SPI bus. It receives phase gradients and attenuation. SPI master module is located in RC which initiates and controls the communication. As shown in figure 4, on trigger 'SPI_TRIG' PGC de-serializes the data and extracts the required gradients. It also provides the starting point for the computation process for further calculations.

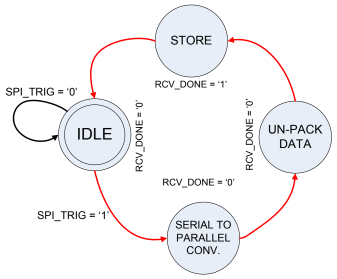

Figure 4: SPI Slave Module State Machine

2) Computation Process: This software module calculates phase attenuation values required for the individual channels. On 'RCV_DONE' trigger from the SPI slave, it performs:

$$Phase\ (n,f) = n * P_A + Ph_{err}(n,f) \qquad \text{(iv)}$$

$$Attn\ (n,f) = Attn'\ (n,f) + Attn_{err}(n,f) \qquad \text{(v)}$$

All the values corresponding to the N channels are computed in parallel. It also provides triggers to the SPI master modules to set the phases & attenuation values for each T/R channel.

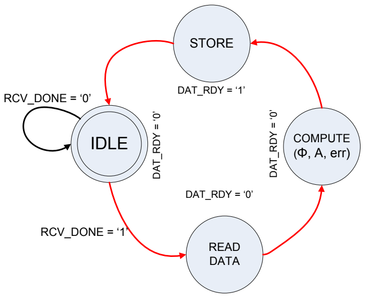

Figure 5: Computation Process Module State Machine

3) SPI Master Modules: There are independent SPI master modules to communicate with a group of T/R modules. On 'DAT_RDY' trigger from the computation process, the values of Phase and Attenuation are transmitted to corresponding T/R serially.

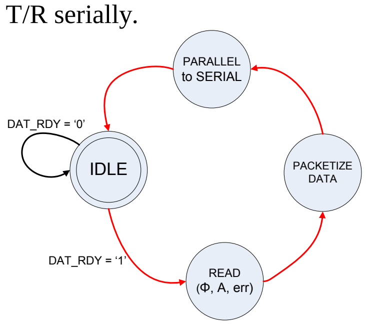

Figure 6: SPI Master Module State Machine

D. *Parameter Update Time*

Radar Controller initiates the communication with PGA over SPI and is configured as Master. Data packets consisting of P_A, P_B, attenuation, mode & frequency are transmitted from RC and in return PGA transmits the data comprising health, temperature & configuration status of each T/R to RC. The data from RC is sent at each Dwell. A data rate of less than 1Mbps is found suitable. A similar communication protocol is established between PGA and T/R modules.

D. *Waveform Simulation*

The simulation result for the proposed design is shown in figure 7. On SPI bus 'SCKI' indicates the input clock and 'SDI' shows the data from RC. Total 42 bit data is received from RC at every 'dwell'. Two signals 'RCV DONE' and 'READY' indicates the states and transition from raw to processed data packets. Signal 'SCKO' indicates the output clock and 'SDO' shows the data from TRC to individual T/R module. Total (18 x 4) bits data are transmitted from PGC to T/R modules.

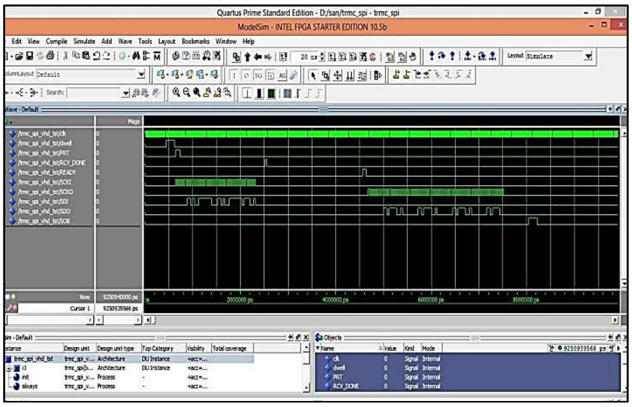

Figure 7: Waveform Simulation Result

V. TEST RESULT

The P_A values corresponding to the azimuth and elevation angles between -45° to +45° is computed. As shown in figure 8, for a given elevation angle, the P_A value rises with increasing azimuth angles.

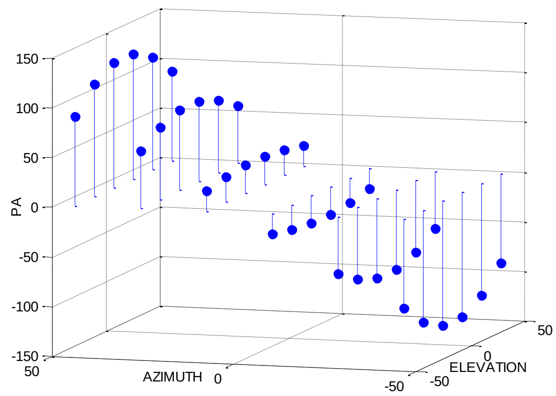

Figure 8: Phase Gradient (P_A) Plot with Azimuth and Elevation Angles

As shown in figure 8, for a given positive azimuth angles, the P_A value is maximum at 0° elevation angle and falls gradually on its either side. For a given negative azimuth angle values, the P_A is minimum at 0° elevation angle and rises on its either side.

The P_B values corresponding to the azimuth and elevation angles between -45° to +45° is computed and is shown in figure 9. For a given positive elevation angles, the P_B value rises with increasing azimuth angles. For a given negative elevation angle values, the P_B value decreases with rising azimuth angles.

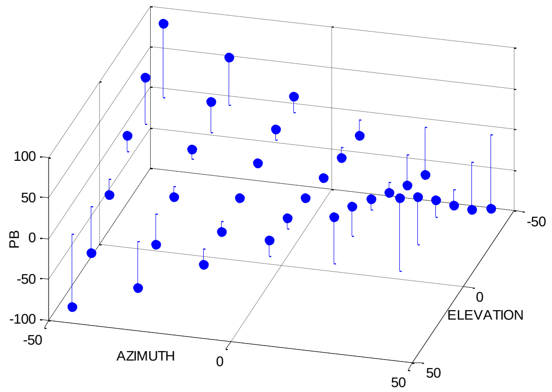

Figure 9: Phase Gradient (P_B) Plot with Azimuth and Elevation Angles

As shown in figure 9, for a given positive azimuth angle values, the P_B value rises with the increasing elevation angles. The P_B value falls with the increasing elevation angles for a given negative azimuth angle values.

The validation results of the proposed design are shown in figure 10 and 11. Signal ‘SCK_RC_IN’ represents the master clock from RC. ‘SDI_RC_OUT’ and ‘SDO_RC_IN’ indicates the data from and to RC respectively.

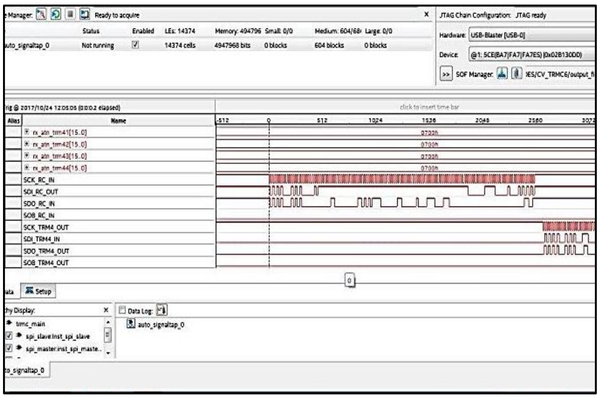

Figure 10: Data Interface between RC and PGC

The computation process is completed and data from one of the T/R module is generated. The signal ‘SCK_TRM4_OUT’, ‘SDI_TRM4_IN’ and ‘SDO_TRM4_OUT’ represents the clock, data out and data input to the PGC respectively.

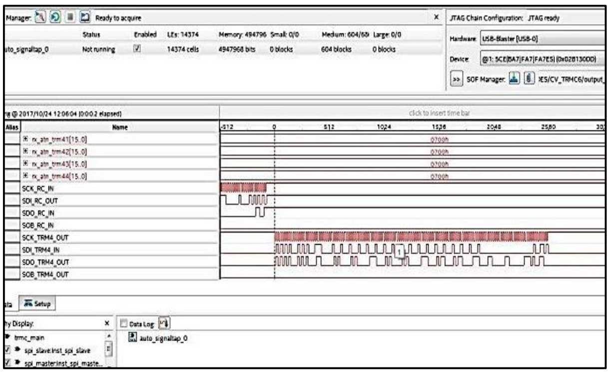

Figure 11: Data Interface between PGC and T/R Module

VI. CONCLUSION

The technology of phased array antenna is widely used in the state of the art Radar systems. The beam steering logic forms an important part of such system. The architecture for computing the phase gradients has been described. The method presented takes common phase angle and derives element specific discrete phase gradients to provide fine control over each antenna element. The simulated results suggest that the timing and distribution delay are well within specification.

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